IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicants(s): Devine et al.
Case: 2-2
Serial No.: 10/787,376
Filing Date: February 26, 2004
Examiner: 2182
Group: Jasjit S. Vidwan

Title: Controller for Peripheral Communications with Processing Capacity for Peripheral Functions

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REPLY BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Appellants hereby reply to the Examiner's Answer, mailed September 14, 2010 (referred to hereinafter as "the Examiner's Answer"), in an Appeal of the final rejection of claims 4, 5, 10, 11, 17, and 18 in the above-identified patent application.

REAL PARTY IN INTEREST

A statement identifying the real party in interest is contained in Appellants' Appeal Brief.

RELATED APPEALS AND INTERFERENCES

A statement identifying related appeals is contained in Appellants' Appeal Brief.

STATUS OF CLAIMS

A statement identifying the status of the claims is contained in Appellants' Appeal Brief.

STATUS OF AMENDMENTS

A statement identifying the status of the amendments is contained in Appellants' Appeal Brief.

SUMMARY OF CLAIMED SUBJECT MATTER

A Summary of the Invention is contained in Appellants' Appeal Brief.

STATEMENT OF GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A statement identifying the grounds of rejection to be reviewed on appeal is contained in Appellants' Appeal Brief.

CLAIMS APPEALED

A copy of the appealed claims is contained in an Appendix of Appellants' Appeal Brief.

ARGUMENT

Points 1-2

Appellants note that the present disclosure provides a Summary of the Invention. The summary presented in Point 2 of the Response to Arguments section of the Examiner's Answer is the *Examiner's interpretation* of the invention. The four basic elements noted by the Examiner do not provide an accurate representation of the *cited claims* and, for example, are missing the requirement for "performing at least one function in addition to said one or more communication functions" of some of the pending claims.

Point 3

The Examiner asserts that the "prior art of Sartore differs from the problem that the Appellant attempts to resolve is on the point that Sartore only includes a single controller responsible for the functions of the device and provide processing capacity for the communications cited for USB interface."

As noted in the Appeal Brief, Sartore provides few details on the peripheral device 54. Contrary to the Examiner's assertion, Sartore does *not* disclose that only a single controller is included or that only a single controller is included that is responsible for the

functions of the device. As noted in the Appeal Brief, Sartore teaches that CPU 72 is only used to reconfigure the peripheral. Sartore does *not* indicate whether or not the peripheral includes other CPU's or controllers, and Sartore does *not* disclose or suggest that CPU 72 performs any task or function other than reconfiguring the peripheral. Sartore does *not* disclose or suggest that CPU 72 performs one or more communication functions and Sartore does *not* disclose or suggest that CPU 72 performs at least one function for said peripheral device in addition to the one or more communication functions.

The Examiner further asserts that a USB interface does not require a presence of a USB controller and asserts that this is the case for Sartore.

Appellants note that, contrary to the Examiner's assertion, Sartore does *not* address the details of the USB interface and does *not* indicate that a USB controller is not required. As noted in the Background of the Invention section of the present disclosure, a conventional peripheral device includes a USB device controller and a dedicated processor.

First Point 4

The Examiner asserts that "Appellant does not argue on the merits of the processor providing communication control."

The Examiner's statement is *not* accurate. Appellant does not argue on the merits of whether the CPU 72 reconfigures the peripheral. As noted in the Appeal Brief, Appellants argue that Sartore does *not* disclose or suggest performing at least one function for said peripheral device *in addition to* said one or more communication functions, and does *not* disclose or suggest *providing* ***processing capacity for use by*** *said peripheral device*, as required by each independent claim.

To reiterate, Sartore does *not* disclose or suggest that CPU 72 performs one or more communication functions and Sartore does *not* disclose or suggest that CPU 72 performs at least one function for said peripheral device in addition to the one or more communication functions.

Second Point 4

The Examiner asserts that:

> Sartore is modifying the processor already present in a peripheral to include functionality of executing a simulated disconnection and reconnection. The said modifications do not require the peripheral device to include an additional processor or alter the embodiment of the peripheral in question.

Therefore, the processor residing on the peripheral will maintain its normal functions without Sartore needing to explicitly state what such functions are.

Contrary to the Examiner's assertion, Appellants find *no* disclosure or suggestion in Sartore that the alleged modifications do not require the peripheral device to include an additional processor. Appellants note that Sartore teaches that CPU 72 reconfigures the peripheral. Sartore does *not* disclose or suggest that CPU 72 includes functionality of executing a simulated disconnection and reconnection. Moreover, Sartore does *not* disclose or suggest that another processor that is 1) present in the peripheral; and 2) includes functionality of executing a simulated disconnection and reconnection is also performing one or more communication functions or providing processing capacity in addition to the simulated disconnection and reconnection.

Point 5

The Examiner asserts that, absent the processor of (the) peripheral providing said processing capacity for the functions of the said peripheral, the only alternative would be for the host to assume such responsibilities.

Contrary to the Examiner's assertion, having the host assume such responsibilities is *not* the only alternative. As noted in the Background of the Invention section of the present disclosure, conventional peripheral devices may include additional processors or controllers to assume such responsibilities. Adams teaching that a digital signal processor performs and controls assigned signal processing functions *without the need to incorporate dedicated ROM and RAM* does *not* solve Sartore's deficiency of *not* disclosing that a processor performs of at least one function for the peripheral device *in addition to* one or more communication functions, and *not* disclosing that the processor *provides* ***processing capacity for use by*** *said peripheral device.*

Appeal Brief Arguments

Independent Claims 5, 11 and 18

Independent claims 5, 11, and 18 were rejected under 35 U.S.C. §103(a) as being unpatentable over Sartore et al. and further in view of Adams et al. With regard to claims 5, 11, and 18, the Examiner asserts that Sartore teaches an integrated controller for use in a peripheral device for controlling high speed communications (citing element 71, FIG. 2) between a host

computer (element 52, FIG. 2) and said peripheral device (element 54, FIG. 2), comprising: a processor (element 72, FIG. 2) integrated with said controller for controlling communications on a bus using one or more communication functions (col. 5, lines 18-23), wherein said processor performs at least one function for said peripheral device in addition to said one or more communication functions (col. 5, lines 25-35).

The Examiner acknowledges that Sartore does not provide details on functions of the peripheral. The Examiner alleges that it would be inherent that the CPU controls at least one function of the peripheral device. The Examiner asserts that Adams teaches a single processor in a peripheral performing functions of the peripheral device.

As discussed hereinafter, the CPU 72 in the peripheral 54 of Sartore does not "perform at least one function for said peripheral device *in addition to* said one or more communication functions," as required by the independent claims. Rather, it is clear that the CPU 72 in Sartore is only used to *reconfigure* the peripheral over a USB interface 71. The CPU 72 is not used for the normal operation of the peripheral.

As indicated in the Abstract of Sartore (emphasis added):

> A system and method for *reconfiguring* a peripheral device connected by a computer bus and port to a host from a *first* generic configuration to a *second* manufacturer specific configuration is provided in which the configuration of a peripheral device may be electronically reset. A peripheral interface device for a standardized computer peripheral device bus and port is also provided in which a physical disconnection and reconnection of the peripheral device is *emulated to reconfigure* the bus and port for a particular peripheral device.

See, also, col. 5, lines 23-25, where it is noted that memory 74 may initially contain an identification code to indicate which *configuration information* set should be *downloaded* to the peripheral device.

Thus, among other limitations, the CPU 72 of Sartore does not disclose or suggest performing at least one function for said peripheral device *in addition to* said one or more communication functions, or *provide* ***processing capacity for use by*** *said peripheral device*, as required by each independent claim.

Adams is cited for a processor in a peripheral for performing and controlling functions of the peripheral. Adams does *not* disclose or suggest a processor *integrated with said controller* for performing at least one function for said peripheral device *in addition to* said one

or more communication functions, or *provide* ***processing capacity for use by*** *said peripheral device*, as required by each independent claim.

In the Response to Arguments section of the final Office Action, the Examiner acknowledges that Sartore is primarily focused on the disclosure with respect to reconfiguring the peripheral device, but asserts that it would be hard to argue that processors for peripheral devices would not be configured to perform at least one function for said peripheral device. The Examiner further asserts that it is widely accepted that, unless specifically stated that the processor of the host computer relieves the peripheral processor of processing capacity, one can confidently assume that the cited processor of peripheral devices is configured to perform functions for the peripheral devices.

Appellants maintain that the cited prior art does *not* disclose or suggest that a processor *integrated with said controller* for performing at least one function for said peripheral device *in addition to* said one or more communication functions. Moreover, the Examiner has provided *no* evidence to support an assertion that "it is widely accepted that, unless specifically stated that the processor of the host computer relieves the peripheral processor of processing capacity, one can confidently assume that the cited processor of peripheral devices are configured to perform functions for the peripheral devices." Appellants note that, were such a statement widely known, there would exist prior art disclosing such a feature.

Thus, Appellants respectfully request that the rejection of the cited claims under 35 U.S.C. §103(a) as being unpatentable over Sartore et al. and further in view of Adams et al. be withdrawn.

Conclusion

The rejections of the cited claims under section 103 in view of Sartore et al. and Adams et al., alone or in any combination, are therefore believed to be improper and should be withdrawn. The remaining rejected dependent claims are believed allowable for at least the reasons identified above with respect to the independent claims.

The attention of the Examiner and the Appeal Board to this matter is appreciated.

Respectfully,

/Kevin M. Mason/

Date: November 15, 2010

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CLAIMS APPENDIX

1. (Cancelled).

2. (Cancelled).

3. (Cancelled).

4. The controller of claim 5, wherein said at least one peripheral device employs said processor to perform each of said functions of said at least one peripheral device.

5. An integrated controller for use in a peripheral device for controlling high speed communications between a host computer and said peripheral device, comprising:

a processor integrated with said controller for controlling communications on a bus using one or more communication functions, wherein said processor performs at least one function for said peripheral device in addition to said one or more communication functions, wherein said processor provides processing capacity for use by said peripheral device, and wherein said high speed communications conform to a USB standard.

6. (Cancelled).

7. (Cancelled).

8. (Cancelled).

9. (Cancelled)

10. The method of claim 11, wherein said at least one peripheral device employs said first processor to perform each of said functions of said at least one peripheral device.

11. A method performed by a controller on a peripheral device for controlling communications between a host computer and said peripheral device, comprising the step of:

executing one or more communication functions that control communications on a bus using a first processor, wherein said first processor also performs at least one function for said peripheral device in addition to said one or more communication functions, wherein said processor is integrated with said controller and provides processing capacity for use by said peripheral device, and wherein said high speed communications conform to a USB standard.

12. (Cancelled).

13. (Cancelled).

14. (Cancelled).

15. (Cancelled).

16. (Cancelled)

17. The integrated circuit of claim 18, wherein said at least one peripheral device employs said processor to perform each of said functions of said at least one peripheral device.

18. An integrated circuit for use in a peripheral device, comprising:

a controller for high speed communications between a host computer and at least one peripheral device, comprising:

a processor integrated with said controller for controlling communications on a bus using one or more communication functions, wherein said processor performs at least one function for said peripheral device in addition to said one or more communication functions, wherein said processor provides processing capacity for use by said peripheral device, and wherein said high speed communications conform to a USB standard.

19. (Cancelled).

20. (Cancelled).

EVIDENCE APPENDIX

There is no evidence submitted pursuant to § 1.130, 1.131, or 1.132 or entered by the Examiner and relied upon by appellant.

RELATED PROCEEDINGS APPENDIX

There are no known decisions rendered by a court or the Board in any proceeding identified pursuant to paragraph (c)(1)(ii) of 37 CFR 41.37.